REMARKS

Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claims 1-14 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant has amended claims 1-14 to more particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Claim Rejections – 35 U.S.C. § 102/103

The Examiner has rejected claims 1, 8, 9 and 12 under 35 U.S.C. § 102(b) as being anticipated by Krivokapic (US Patent 5,824,587). The Examiner has rejected claim 13 under 35 U.S.C. § 102(e) as being anticipated by Takeuchi (US Patent 5,970,351). The Examiner has rejected claim 15 under 35 U.S.C. § 102(e) as being anticipated by Choi (US Patent 6,057,582). The Examiner has rejected claim 2 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic (US Patent 5,824,587) in view of Takeuchi (US Patent 5,970,351). The Examiner has rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 as applied to claim 1 above and further in view of Choi '582. The Examiner has rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi '582. The Examiner has rejected claims 5 and 6 under 35 U.S.C. § 103(a) as being unpatentable over Krivokapic '587 in view of Choi et al. (US Patent 5,793,088). The Examiner has rejected claims 7, 10 and 11 under 35 U.S.C. § 103(a) as being unpatentable

over Krivokapic '587. The Examiner has rejected claim 14 under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi '351 in view of Choi '582.

With respect to claims 1-10, Applicant teaches and claims a MOS transistor having a gate electrode formed on a gate dieletric layer and a pair of source/drain regions. The source/drain regions are inwardly concaved and create an inflection points (260, Figure 2) beneath the gate electrode 202 and gate dielectric layer 204. That is, Applicant teaches and claims an MOS transistor structure which has source/drain regions which create inflection points which are located beneath the gate dielectric layer 204 formed beneath the gate electrode 202.

It is applicant understanding that Krivokapic describes a transistor 300 (Figure 2P) which has a pair of source/drain regions 217 and 218. It's Applicant's understanding that the ion-implantation process used to form the source/drain regions 217 and 218 would not form inwardly concaved source/drain structures nor would it created inflections points as claimed by Applicant. Even if, for argument sake, source/drain regions 217 and 218 were inwardly concaved and create inflections points, the inflection points of the source and drain regions do not reside beneath the gate dielectric layer and gate electrode as claimed by Applicant. As shown in Figure 2o, the inflection point would reside below spacer 219 and pad oxide layer 202 and not below gate electrode 210 and gate dielectric layer 208 as claimed by Applicant. See, for example, Figure 2o where the point of the source and drains regions which are closest together, resides beneath spacer 219 and not gate electrode 210 and gate dielectric 208 as claimed by Applicant.

With respect to claims to 2-12, neither Takeuchi nor Choi teach source/drain structures as claimed by Applicant. As such, claims 2-12 are allowable for at least the reasons of claim 1.

Additionally, with respect to claims 3 and 4, Applicant further claims that the gate dielectric layer is thicker beneath the outside edge of the gate electrode than the gate dielectric layer beneath the center of the gate electrode. It is Applicant's understanding that one of ordinary skill in the art would not combine Choi's dielectric film 22 with the transistor

structure of Krivokapic because the processes used to form Krivokapic transistor and Choi's gate dielectric are incompatible. That is, as shown in Figure 3D and 4D of Choi, the thicker dielectric layer 22 is formed by forming a protrusion in the gate electrode layer which is able to bend upwardly in order to form a thick gate dielectric layer 22. Applicant does not understand how such a process would be implemented into the process described in Krivokapic. As such, one of ordinary skill in the art would not combine the two references. Accordingly, claims 3 and 4 are allowable for at least this reason also.

With respect to claims 13, Applicant claims an MOS device having a gate dielectric layer and a gate electrode. The MOS device includes a pair of silicon germanium alloy source/drain regions having a second conductivity type formed in the substrate along opposite sides of the gate electrode wherein the silicon germanium alloy source/drain regions in said substrate are inwardly concaved and create inflection points in said substrate. Applicant does not understand Takeuchi to teach silicon germanium source/drain regions formed in a substrate which are inwardly concaved and create an inflection point as claimed by Applicant. As such, Applicant respectfully requests the removal of the 35 U.S.C. § 102(e) rejections of claim 13 and seeks an early allowance of this claim.

With respect to claim 14, claim 14 depends upon claim 13 and as such is allowable for at least the reasons of claim 13.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

1. (Amended) An MOS device comprising:

a gate dielectric formed on first conductivity region **[in]** **of** a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of **[deposited]** silicon or silicon alloy **inwardly concaved** source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode **and creating inflection points beneath said gate electrode and said gate dielectric layer**, wherein said silicon or silicon alloy source/drain regions extend beneath the gate electrode and define a channel region beneath said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said gate electrode is larger than said channel region **[deeper into said first conductivity type region]** **between said inflection points**.

5. (Amended) The MOS device of claim 1 further comprising a pair of **[deposited]** silicon or silicon alloy regions having a first conductivity type **region** formed between said pair of **[deposited]** silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region.

6. (Amended) The MOS device of claim 5 wherein the concentration of said **[deposited]** silicon or silicon alloy regions having a **first** conductivity type is greater than the concentration of said first conductivity type region.

7. (Amended) The MOS device of claim 1 wherein said **[deposited]** silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said gate electrode at **[an]** **said** inflection **[point]** **points** which occurs **[of]** between 50-250Å laterally beneath said gate electrode and at a depth of between 25-200Å beneath said gate dielectric.

10. (Amended) The MOS device of claim 1 wherein the concentration of said **[deposited]** silicon or silicon alloy source/drain regions of a second conductivity type have a concentration between $1x10^{18}/cm^3 - 3x10^{21}/cm^3$.

11. (Amended) The MOS device of claim 10 wherein the concentration of said **[deposited]** silicon or silicon alloy source/drain regions of a second conductivity type is approximately $1x10^{21}/cm^3$.

12. (Amended) The MOS device of claim 1 further comprising silicide formed on said **[deposited]** silicon or silicon alloy source/drain regions.

13. (Amended) An MOS device comprising:

a gate dielectric formed on a first conductivity type region **[in]** **of** a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of **[deposited silicon or silicon alloy]** **silicon-germanium alloy** source/drain regions having a second conductivity type formed in said substrate and along opposite sides of said gate electrode wherein said **[deposited silicon or silicon alloy]** **silicon-germanium alloy source/drain region in said substrate are inwardly concaved and create an inflection point in said substrate, said silicon germanium alloy** extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon or silicon alloy is

spaced further from said gate electrode than said silicon or silicon alloy adjacent to said gate dielectric.